WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a first controlling circuit section inputted with an input signal having amplitude between a low voltage and the ground, operating with the low voltage of electricity source, putting out a first control signal generated by said input signal, putting out an inverse signal of the first control signal, and putting out a second control signal generated from the first control signal,

a level transforming circuit inputted with said first control signal, inputted with said inverse signal, putting out a first signal having amplitude between said low voltage and a high voltage higher than said low voltage,

a first buffer circuit which has first p-channel type MOS transistor connected between said high voltage of electricity source and first output node, impressed gate of said first p-channel type MOS transistor with said first control signal, and which has first n-channel type MOS transistor connected between said first output node and the ground, impressed gate of said first n-channel type MOS transistor with said first control signal, and wherein said first buffer circuit puts out a second signal having amplitude between said high voltage and said low voltage to said first output node;

a second buffer circuit which has second p-channel type MOS transistor connected between said low voltage of electricity source and second output node, impressed gate of said second p-channel type MOS transistor with said second control signal, and which has second n-channel type MOS transistor connected between said second output node and the ground, impressed gate of said second n-channel type MOS transistor with said second control signal, and wherein said

second buffer circuit puts out a third signal having amplitude between said low voltage and the ground to said second output node; and

a overvoltage protecting circuit which has third p-channel type MOS transistor connected drain of said third p-channel type MOS transistor with third output node, impressed source of said third p-channel type MOS transistor with said second signal, and which has third n-channel type MOS transistor connected drain of said third n-channel type MOS transistor with third output node, impressed source of said third n-channel type MOS transistor with said third signal, and wherein said overvoltage protecting circuit impressed each gate of said third p-channel type MOS transistor and said third n-channel type MOS transistor with said low voltage in common, puts out a fourth signal having amplitude between said high voltage and the ground to said third output node.

2. A semiconductor integrated circuit according to Claim 1: further comprising

a pre-buffer circuit connected with the output of said level transforming circuit, so as to put out said first signal having amplitude between the high voltage and the low voltage.

3. A semiconductor integrated circuit according to Claim 2: wherein

said pre-buffer circuit adjusts timing of inputting said first buffer circuit with said first signal.

4. A semiconductor integrated circuit according to Claim 1: wherein

turning on resistance of said first p-channel type MOS transistor in said first buffer circuit is set higher than turning on resistance of said third p-channel type MOS transistor, and

turning on resistance of said second n-channel type MOS transistor in said second buffer circuit is set higher than turning on resistance of said third n-channel type MOS transistor in said overvoltage protecting circuit.

5. A semiconductor integrated circuit according to Claim 1: wherein

substrates of said first n-channel type MOS transistor in said first buffer circuit is connected with source of said first n-channel type MOS transistor, and substrate of said third n-channel type MOS transistor in said overvoltage protecting circuit is connected with source of said third n-channel type MOS transistor; isolated from substrate of said second n-channel type MOS transistor.

6. A semiconductor integrated circuit according to Claim 1: wherein

substrate of said third p-channel type MOS transistor is connected with source of said third p-channel type MOS transistor, isolated from substrates of said first and second p-channel type MOS transistor.

7. A semiconductor integrated circuit according to Claim 1: wherein

said p-channel type MOS transistors and said n-channel type MOS transistors are formed on an active region isolated by insulating film.

8. A semiconductor integrated circuit comprising:

a first controlling circuit section inputted with a data input signal having amplitude between a low voltage and the ground, inputted with an enable signal, operating with the low voltage of electricity source, putting out a first control signal generated by said data input signal and said enable signal, putting out a first inverse signal of the first control signal, putting out a second control signal generated by said data input signal and said enable signal, putting out a second

inverse signal of the second control signal, putting out a third control signal generated from the first control signal, and putting out a fourth control signal generated from the second control signal,

a first level transforming circuit inputted with said first control signal, inputted with said first inverse signal, putting out a first signal having amplitude between said low voltage and a high voltage higher than said low voltage,

a second level transforming circuit inputted with said second control signal, inputted with said second inverse signal, putting out a second signal having amplitude between said low voltage and a high voltage higher than said low voltage,

a first buffer circuit which has first p-channel type MOS transistor impressed gate of said first p-channel type MOS transistor with said first control signal, connected between said high voltage of electricity source and first output node, and which has first n-channel type MOS transistor impressed gate of said first n-channel type MOS transistor with said second control signal, connected between said first output node and the ground, and wherein said first buffer circuit puts out a third signal having amplitude between said high voltage and said low voltage to said first output node;

a second buffer circuit which has second p-channel type MOS transistor impressed gate of said second p-channel type MOS transistor with said third control signal, connected between said low voltage of electricity source and second output node, and which has second n-channel type MOS transistor impressed gate of said second n-channel type MOS transistor with said fourth control signal, connected between said second output node and the ground, and wherein said second buffer circuit puts out a fourth signal having amplitude between said low voltage and the ground to said second output node; and

a overvoltage protecting circuit which has third p-channel type MOS transistor impressed source of said third p-channel type MOS transistor with said third signal, connected drain of said third p-channel type MOS transistor with third output node, and which has third n-channel type MOS transistor impressed source of said third n-channel type MOS transistor with said fourth signal, connected drain of said third n-channel type MOS transistor with third output node, and wherein said overvoltage protecting circuit impressed each gate of said third p-channel type MOS transistor and said third n-channel type MOS transistor with said low voltage in common, puts out a fifth signal having amplitude between said high voltage and the ground to said third output node.

9. A semiconductor integrated circuit according to Claim 8: further comprising

a pre-buffer circuit connected with the output of said first level transforming circuit, so as to put out said first signal having amplitude between the high voltage and the low voltage.

10. A semiconductor integrated circuit according to Claim 9: wherein

said pre-buffer circuit adjusts timing of inputting said first buffer circuit with said first signal.

11. A semiconductor integrated circuit according to Claim 8: wherein

turning on resistance of said first p-channel type MOS transistor in said first buffer circuit is set higher than turning on resistance of said third p-channel type MOS transistor, and

turning on resistance of said second n-channel type MOS transistor in said second buffer circuit is set higher than turning on resistance of said third n-channel type MOS transistor in said overvoltage protecting circuit.

12. A semiconductor integrated circuit according to Claim 8: wherein

substrates of said first n-channel type MOS transistor in said first buffer circuit is connected with source of said first n-channel type MOS transistor, and substrate of said third n-channel type MOS transistor in said overvoltage protecting circuit is connected with source of said third n-channel type MOS transistor; isolated from substrate of said second n-channel type MOS transistor.

13. A semiconductor integrated circuit according to Claim 8: wherein

substrate of said third p-channel type MOS transistor is connected with source of said third p-channel type MOS transistor, isolated from substrates of said first and second p-channel type MOS transistor.

14. A semiconductor integrated circuit according to Claim 8: wherein

said p-channel type MOS transistors and said n-channel type MOS transistors are formed on an active region isolated by insulating film.